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Each core type comes in versions for encryption and decryption, and offers support for any of the AES key sizes (128-, 192- and 256-bits), either separately or in combination. Our cores are available in versions specifically aimed at a number of target technologies; generic RTL source code for use in ASICs, and highly optimised netlists for use with Altera, Lattice, Microsemi (Actel) and Xilinx FPGA technology.

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IP core offering to Altera FPGA users]], says Jean-Francois Nivart, CSO of intoPIX. "Our Altera IP-cores will address the increasing customer demand for our high performance JPEG 2000 real-time encoder and decoder cores and directly benefit from the access to the fast growing Altera market share."

intoPIX - PR -JPEG2000 IP cores on Altera FPGA Devices

Intel FPGA and its Intellectual Property partners offer a large selection of off-the-shelf IP cores and reference designs optimized for Intel FPGA, CPLD, and ASIC devices. These IP solutions can be used to accelerate design development and reduce project

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The AES-P IP core implements the FIPS-197 Advanced Encryption Standard. It can be programmed to encrypt or decrypt 128-bit blocks of data, using 128-, 192-, or 256-bit cipher-key. The Block Cipher mode of operation is run-time programmable to ECB, CBC, CFB, OFB, or CTR.

Programmable Block Cipher Mode AES IP Core

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The SHA256 IP core is a high performance implementation of the SHA-256 Message Digest algorithm, a one-way hash function, compliant with FIPS 180-2. The core is composed of two main units, the SHA256 Engine and the Padding Unit as shown in the block diagram. The SHA256 Engine applies the SHA256 loops on a single 512-bit message block, while the Padding Unit splits the input message into 512-bit blocks and performs the message padding on the last block of the message.

SHA-256 IP Core Secure Hash Function - Alma Technologies

Altera AES IP Cores perform data encryption and/or decryption as specified by the Federal Information Processing Standard (FIPS) 197, Advanced Encryption Standard (AES).

Altera AES IP Core - Design And Reuse

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The AES core implements Rijndael cipher encoding and decoding in compliance with the NIST Advanced Encryption Standard. It processes 128-bit data blocks with 128-bit key (a 256-bit key version is available). Basic core is designed only for encryption and is the smallest available on the market (less than 3,000 gates).

AES IP Core: Ultra-Compact Advanced Encryption Standard ...

2.1. Installing and Licensing Intel FPGA IP Cores. The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use.